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Reconsideration of this application, as amended, is respectfully requested.

Claims 12-17 and 23-36 were pending. Claims 23-36 have been allowed. Claims 12-17 have been rejected.

Claim 1 has been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicant submits that the amendments do not add new matter.

**ALLOWABLE SUBJECT MATTER**

Applicant notes with appreciation the Examiner's allowance of the claims 23-36.

**REJECTIONS UNDER 35 U.S.C. § 103**

Claims 12-17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,495,467 to Shin, et al. ("Shin"), in view of U.S. Patent No. 5,091,326 to Haskell ("Haskell"), further in view of U.S. Patent No. 5,734,607 to Sung et al. ("Sung"). Applicant has amended claim 12 to include a single one-dimensional slot patterned in the ILD to provide access to the plurality of active regions; and a bit line formed in the single slot to contact the active regions, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width.

The Examiner acknowledged that "Shin et al. fail to disclose the required slot/pattern in interlayer dielectric and the required bit lines" (Office Action, 08/14/06, p.2).

Haskell discloses fabricating contacts for EPROM elements. More specifically, Haskell discloses etching the plurality of interconnect areas using a slot mask having the plurality of slots (col. 5, lines 59-65, Figures 4a, 4b, and 5b).

Sung discloses a method of manufacturing of a self-aligned bit-line. More specifically, Sung discloses forming a plurality of openings down to the drains to the surface of the drain regions (col. 4, lines 65-67). In particular, Sung discloses that a bit-line is formed across the gate stacks to contact the drain regions through the plurality of openings (col. 5, lines 4-20). In contrast, amended claim 1 refers to a single one-dimensional slot patterned in the ILD to provide access to the plurality of active regions. A bit line is formed in the single slot to contact the active regions, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width.

It is respectfully submitted that Shin does not teach or suggest a combination with Haskell and Sung, Haskell does not teach or suggest a combination with Shin and Sung, and Sung does not teach or suggest a combination with Shin and Haskell. Shin teaches a U-shaped floating gate to increase coupling to a control gate. Haskell, in contrast, teaches fabrication of contacts to EPROM elements. Sung, in contrast to Shin and Haskell, teaches forming the self-aligned bit line. It would be impermissible hindsight based on Applicants' own disclosure, to combine Shin, Haskell, and Sung.

Furthermore, even if Shin, Haskell, and Sung were combined, such a combination would lack a single one-dimensional slot patterned in the ILD to provide access to the plurality of active regions; and a bit line formed in the single slot to contact the active regions, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width.

Therefore, Applicants respectfully submit that amended claim 12 is not obvious under 35 U.S.C. § 103(a) over Shin, in view of Haskell, and further in view of Sung.

Because claims 13-17 depend from amended claim 12, and add additional limitations, Applicants respectfully submit that claims 13-17 are not obvious under 35 U.S.C. § 103(a) over Shin, in view of Haskell, and further in view of Sung.

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CONCLUSION


It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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